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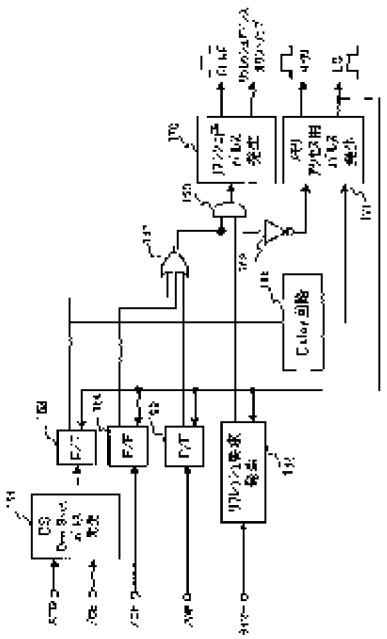
(54) SEMICONDUCTOR STORAGE DEVICE

(57) Abstract:

PROBLEM TO BE SOLVED: To periodically carry out refresh of a memory cell by a refresh timer and to avoid the contention between a memory access and memory refresh.

SOLUTION: When a memory access is made, a F/F163 is set by a one shot pulse from an OS circuit 161, a memory access request is inputted into a memory access pulse generating circuit 171 through a NOR gate 167 and a latch control signal LC and an enable signal REN are outputted. When a refresh request is inputted into an AND gate 168 from the refresh timer and it is making memory access, the output of the NOR gate 167 becomes an 'L' level and the refresh request is blocked by the AND gate 168. After that, when the signal LC becomes an 'L' level, F/Fs 163, 164 and 165 are reset, the output of the NOR gate 167 becomes an 'H' level, the refresh request is inputted into a refresh pulse generating circuit 170 and a refresh enable signal RERF is outputted.

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